Application No.: 10/660,855   2   Docket No.: 404332000101

AMENDMENTS TO THE CLAIMS

1-3.   (canceled)

4. (new) A computer system comprising:

a plurality of first subsystems; and

a second subsystem;

wherein each first subsystem includes multiple processing elements intra-connected to permit communication within such first subsystem among the processing elements;

wherein each first subsystem includes at least one processing element that is coupled as a respective communication and processing unit for such respective first subsystem which permits communication among the multiple processing elements of such first subsystem and processing elements of another first subsystem coupled to serve as a communication and processing unit for the second subsystem; and

wherein the second subsystem includes the plurality of first subsystems; and

wherein multiple processing elements of the another first subsystem that is coupled to serve as a communication and processing unit for such second subsystem are coupled to permit communication among the at least one processing elements of the multiple respective first subsystems that are coupled to serve as communication and processing units for their respective first subsystems.

5. (new) The computer system of claim 4,

wherein there is a first proportionality between a number of processing elements in each of the multiple first subsystems to a number of processing elements in the first subsystems that are coupled to serve as a communication and processing units; and

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wherein there is a second proportionality between a number of first subsystems in the second subsystem and a number of first subsystems that are coupled to serve as a communication and processing units; and

wherein the first proportionality substantially equals the second proportionality.

6. (new) The computer system of claim 4,

first and second second subsystems; and

a third subsystem;

wherein the third subsystem includes the first and second second subsystems, and at least two additional first subsystems that are coupled to serve as communication and processing units for such third subsystem; and

wherein multiple respective processing elements of the at least two additional first subsystems are coupled to permit communication among multiple respective at least one processing elements of multiple respective first subsystems of the first and second second subsystems that are coupled to serve as communication and processing units for their respective first subsystems.

7. (new) The computer system of claim 4,

wherein there is a first proportionality between a number of processing elements in each of the multiple first subsystems to a number of processing elements in the first subsystems that are coupled to serve as a communication and processing units; and

wherein there is a second proportionality between a number of first subsystems in the second subsystem and a number of first subsystems that are coupled to serve as a communication and processing units;

wherein there is a third proportionality between a number of first subsystems in the third subsystem and a number of first subsystems that are coupled to serve as communication and processing units; and

wherein the first, second and third proportionalities are substantially equal to each other.

8. (new) The computer system of claim 4,

wherein each processing element includes a field programmable logic array.

9. (new) The computer system of claim 4,

wherein each processing element includes a field programmable logic array (FPGA); and

wherein a plurality of the FPGAs include associated memory modules.

10. (new) A computer system comprising:

a plurality of first subsystems;

wherein each of the plurality of first subsystems includes multiple processing elements intra-connected to permit communication among the respective processing elements within such at least one network of processing elements; and further including,

first, second, third and fourth blocks of first subsystems;

wherein the first subsystems of the first block are intra-connected to permit intra-communication among the first subsystems within the first block;

wherein the first subsystems of the second block are intra-connected to permit intra-communication among the first subsystems within the second block;

wherein the first subsystems of the third block are intra-connected to permit intra-communication among the first subsystems within the third block; and

wherein the first subsystems of the fourth block are intra-connected to permit intra-communication among the first subsystems within the fourth block; and further including,

a **first first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the **first block** and respective first subsystems of the **second block**;

a **second first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the **first block** and respective first subsystems of the **third block**;

a **third first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the **second block** and respective first subsystems of the **third block**; and

a **fourth first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the **third block** and respective first subsystems of the **fourth block**.

11. (new) The computer system of claim 10,

wherein at least one processing element of each of multiple respective first subsystems of the **first block** is coupled to serve as a communication and processing unit for its respective first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **first first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the first block and respective subsystems of the second block;

wherein at least one processing element of each of multiple respective first subsystems of the **second block** is coupled to serve as a communication and processing unit for its respective first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **first first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the first block and respective subsystems of the second block;

wherein at least one processing element of each of multiple respective first subsystems of the **third block** is coupled to serve as a communication and processing unit for its respective first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **second first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the third block and respective subsystems of the fourth block;

wherein at least one processing element of each of multiple respective first subsystems of the **fourth block** is coupled to serve as a communication and processing unit for its respective first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **second first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the third block and respective subsystems of the fourth block;

wherein at least one processing element of each of multiple respective first subsystems of the **first block** is coupled to serve as a communication and processing unit for its respective first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **third first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the first block and respective subsystems of the fourth block;

wherein at least one processing element of each of multiple respective first subsystems of the **fourth block** is coupled to serve as a communication and processing unit for its respective

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first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **third first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the first block and respective subsystems of the fourth block;

wherein at least one processing element of each of multiple respective first subsystems of the **second block** is coupled to serve as a communication and processing unit for its respective first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **fourth first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the second block and respective subsystems of the third block; and

wherein at least one processing element of each of multiple respective first subsystems of the third block is coupled to serve as a communication and processing unit for its respective first subsystem so as to permit communication among the multiple processing elements of its respective first subsystem and processing elements of the **fourth first** subsystem that is coupled to serve as a communication and processing unit for inter-communication between respective first subsystems of the second block and respective subsystems of the third block.

12. (new) The computer system of claim 10,

wherein each processing element includes a field programmable logic array.

13. (new) The computer system of claim 10,

wherein each processing element includes a field programmable logic array (FPGA); and

wherein a plurality of the FPGAs include associated memory modules.

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